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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,415	10/23/2003	David W. Boerstler	AUS920030369US1	8491

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EXAMINER	
LEJA, RONALD W	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 12/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/692,415	BOERSTLER ET AL.	
	Examiner	Art Unit	
	Ronald W Leja	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim 12 is objected to because of the following informalities: There is a lack of antecedent basis for "the same fuse blow control signal input" in Claim 12. Appropriate correction is required.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-5, 7-10, 13-23 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Colclaser et al. (6,327,125).

Colclaser et al. disclose, in Figure 1, a system for decoupling a capacitive path (26,24) from an IO pad (51,52) and a protected component (60) utilizing a first fuse (45) and a second fuse (40) (for Claims 3, 17, 18). The IO pad (51,52) are considered to have a source a current via signaling received for protected circuit (60). Pin (73) and pin (76) are considered to be fuse blow pads (for Claim 4), which receive control signals (Claim 5) of either a high potential or ground potential so as to conduct current through the first and/or second fuse, thereby decoupling the associated capacitive paths. The capacitive paths comprise esd protective circuits comprised of diodes (for Claims 7-9, 14). See also, Abstract, Col. 1, lines 30-32; Col. 2, lines 7-16; Col. 3, lines 44-57; Col. 4, line 25 thru Col. 5, line 2.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 2, 11, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Colclaser et al..

Claim 2 adds that the protected component is a processor and Claim 11 adds that the difference between a voltage applied to the IO pad and the ground voltage is less than the activation voltage of the first or second diode. Colclaser et al. refer to the protected component as being an RF circuit and does not specifically recite that the protected component can be a processor or that the difference between a voltage applied to the IO pad and the ground voltage is less

than the activation voltage of the first or second diode. However, it is the opinion of the Examiner that it would have been obvious to apply the teachings of Colclaser et al. to any integrated circuit or pcb circuitry needing esd protection, such as processors, and to eliminate the esd protection upon insertion of the chip or board into a system (when such devices are less susceptible to esd events) so as to increase signal speed. Processor speed is often a critical feature in any circuit design. As far as the difference between the voltages, it is clear that when the fuse is being blown, the conduction of the esd protection circuitry is not necessary, therefore, it would have been obvious to only use a voltage difference sufficient enough to blow the fuse and avoid any unnecessary triggering of the esd/(diodes), which could create other problems. This would help ensure design functional reliability. Claims 24 and 25 add a plurality of protected circuits. It is the opinion of the Examiner that it would have been obvious to apply the teachings of Colclaser et al. to any integrated circuit or pcb circuitry needing esd protection, such as those having a plurality of components needing protection, and to eliminate the esd protection upon insertion of the chip or board into a system (when such devices are less susceptible to esd events) so as to increase signal speed, supra.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Colclaser et al. as applied to Claims 1, 7 and 11 above, and further in view of Bertin et al. (6,141,245).

Claim 12 adds a plurality of fuse blow control devices connected to the same fuse blow control signal input. Colclaser et al. teach the use of a single control device/(voltage supplier) per control signal input (73,76). However, Bertin et al. teach (see Figure 2b) a fuse blowing scheme, wherein more than one fuse blow control device (80a') and (80a) are connected to the same fuse blow control signal input (60). It would have been obvious to apply the teachings of Bertin et al. as a means to allow for a more tailored capacitive path decoupling, thereby increasing the number of applications for the overall chip or pcb circuit. This results in lower manufacturing costs for different applications.

Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Colclaser et al. as applied to Claims 1 and 3 above, and further in view of Aipperspach et al. (6,509,236).

Claim 29 adds the use of a laser for blowing the fuse. Colclaser et al. are somewhat silent with respect to laser fuse blowing. However, Aipperspach et al. teach that it is known to utilize a laser for fuse blowing. It would have been obvious to implement as a means to avoid damage from voltages often associated with fuse blowing via biasing, thereby increasing durability.

Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bertin et al. (6,141,245).

Claims 26-28 essentially add the use of applying a voltage to the IO pad of the protected circuit and generating a current between the pad and a control device for capacitive decoupling; Claims 27 and 28

further add the use of computer code for generating a current between the IO pad and the control device. Colclaser et al. are somewhat silent with respect to the use of the IO pad and computer code. Bertin et al. teach the use of the IO pad (see Figure 1) and the use of an external logic or control device for generating the control signal (see Col. 5, lines 1-10). It would have been obvious to apply the teachings of Bertin et al. as a means to offer a highly selective capacitive path trimming (multiple selective path decoupling with respect to same IO pad) and allow for such to be performed via a programmed controller, which adds precision and less manual work by the technician after chip or pcb circuitry is implanted into the system (at a time when esd protection is not as critical and operating speed needs to be increased for performance issues).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ronald W Leja whose telephone number is (571)272-2053. The examiner can normally be reached on Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571)272-2800. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ronald W Leja
Primary Examiner
Art Unit 2836

12/8/04

rwl
December 8, 2004